

Attorney Docket No. 200310842-1; Ser. No. 10/772,945

REMARKS

Reconsideration of the application as amended is respectfully requested.

The Examiner's communication dated Sept. 8, 2005, which includes making the restriction requirement final, is acknowledged.

Claims 1 – 57 are pending. Of these, claims 2, 12 – 15, 17 – 25, 36, 37, 42 – 46, and 50 – 54 are withdrawn from consideration under the restriction requirements. Claims 18 – 19, 26 – 35, 38 – 41, 47 – 49, and 55 – 57 stand rejected under 35 USC § 112. Claims 1, 3, 11, and 16 stand rejected as anticipated under 35 USC § 102. Claims 4 – 10, 26 – 35, 38 – 41, 47 – 49, and 55 – 57 stand rejected for obviousness under 35 USC § 103.

By the present amendment, claims 7, 34, and 35 are canceled, claims 1, 16, 26, 38, 47, and 55 are amended, and new claims 58 - 59 are added. After this amendment, claims 1 – 6, 8 – 33 and 36 – 59 are pending, and claims 2, 12 – 15, 17 – 25, 36, 37, 42 – 46, and 50 – 54 remain withdrawn from consideration.

Amendments of the specification

The specification is amended to properly identify a related case. The title is amended as required by the Examiner. Applicants respectfully submit that the title as amended is indicative of the invention to which the amended claims are directed. A substitute sheet for page 1 is attached hereto.

Rejections under 35 USC § 112

Claims 18 – 19, 26 – 35, 38 – 41, 47 – 49, and 55 – 57 stand rejected under 35 USC § 112. The Examiner's remark that claims 18 – 19 are held to be indefinite is presumed to be moot due to those claims' withdrawal from consideration under the earlier restriction requirements.

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The Examiner's remarks regarding claims 4 and 7 are acknowledged. Rejection of claim 4 under 35 USC § 112 is respectfully traversed. Claim 4 recites, in pertinent part: "wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells." Enabling support for this limitation of claim 4 is found in the specification as filed at page 6 lines 23 – 29 (last ten lines of paragraph [0031] of the published application, US 2005/0167787 A1).

Claims 7, 34, and 35 are canceled without prejudice by the present amendment.

Claims 26, 38, 47, and 55 are amended herein as independent claims. Basis for the insertions in these claims is found in the specification as filed at page 15 line 1 – page 18 line 23 (paragraphs [0055] – [0064] of the published application), in FIG. 16 as filed, and in claims 20, 37, 42, and 50 respectively as filed. These amendments remove the dependence upon non-elected claims that was the reason for rejection of claims 26 – 35, 38 – 41, 47 – 49, and 55 – 57. Therefore, withdrawal of the rejections under 35 USC § 112 and allowance of claims 4, 26 – 33, 38 – 41, 47 – 49, and 55 – 57 are respectfully requested.

Rejections under 35 USC § 102

Claims 1, 3, 11, and 16 stand rejected under 35 USC § 102 as anticipated by Lancaster et al. (US Pat. No. 5,656,837). Claims 1 and 16 are amended herein to more clearly state and distinctly claim what the applicants believe to be their invention. Basis for the limitation inserted in both claims 1 and 16 is found in FIG. 3 (in which the two terminals comprise row conductor 30 and column conductor 40), in FIGS. 14 and 15 as filed, and in the specification as filed at page 9 lines 3 -11 and at page 13 lines 7 – 31 (paragraphs [0039], [0051], and [0052] of the published application, US 2005/0167787 A1). New dependent claims 58 and 59 are supported by the same basis.

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Claim 1 as amended recites (emphasis added):

"A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a *two-terminal* memory cell disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich insulator."

Similarly, claim 16 as amended recites (emphasis added):

"A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a *two-terminal* memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator."

Each cell of the flash memory array of Lancaster et al. consists of devices having at least three terminals – source, drain, and gate (e.g., Lancaster et al., FIGS. 1 and 2). Such devices are discussed in the "BACKGROUND" section of applicants' specification at page 2 line 30 through page 3 line 9 (paragraph 008 of the published application, US 2005/0167787 A1). Removal of any one of the three terminals (source, drain, or gate) of the devices of Lancaster et al. would render their memory array inoperative. Thus, the two-terminal memory cell of applicants' claims 1 and 16 is clearly distinguished from Lancaster et al.

Therefore, withdrawal of the rejections under 35 USC § 102 of claims 1 and 16 and their dependent claims is respectfully requested. Allowances of

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new dependent claims 58 and 59 are respectfully requested for the same reasons.

Rejections under 35 USC § 103 traversed

Claims 4 – 10, 26 – 35, 38 – 41, 47 – 49, and 55 – 57 stand rejected under 35 USC § 103 as being unpatentable over Lancaster et al. (US Pat. No. 5,656,837). Applicants respectfully submit that the Examiner has not presented a *prima facie* case of obviousness under 35 USC § 103. Regarding claim 4, the Examiner states without evidence that it would have been obvious “to use a silicon-rich insulator of each memory cell being electrically isolated from the silicon-rich insulators of all other memory cells in Lancaster et al.’s device in order to use the device in an application which requires various types of storage elements.” Regarding claims 5 – 10, the Examiner states without evidence that it would have been obvious “to use a control element of each memory cell comprises (sic) a tunnel junction, and the storage element of each memory cell comprises (sic) an anti-fuse, a fuse, a tunnel junction, a state-change layer, a chalcogenide, in Lancaster et al.’s device in order to use known memory control and storage elements, of which official notice is taken.” Again, no evidence at all from the prior art of record is presented for either of these statements of obviousness. The same remark applies equally to presumed obviousness of claims 26 – 35, 38 – 41, 47 – 49, and 55 – 57. If the Examiner is making use of facts within his personal knowledge in these rejections, applicants respectfully request an affidavit under 37 CFR 1.104(d)(2). Since no *prima facie* case of obviousness has been made, applicants respectfully request that all the rejections under 35 USC § 103 be withdrawn and that claims 4 – 8, 9, 10, 26 – 33, 38 – 41, 47 – 49, and 55 – 57 be allowed. (Claims 7, 34, and 35 are canceled herein.)

Applicants expressly reserve the right to file divisional and/or continuation applications with any of the canceled or non-elected claims, or

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with similar claims, or with claims to any subject matter disclosed in the present application or incorporated by reference.

This response is believed to be fully responsive to each issue raised in the office action, but if the Examiner maintains any rejection, applicant would appreciate a more detailed explanation of precisely where in the references a particular combination is suggested and the relevant limitations are disclosed.

Applicants believe that the claims as amended are patentable over the prior art and that the application is now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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